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Design of Low Power Vedic Multiplier Based Reconfigurable Fir Filter for DSP Applications

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Abstract
Recent advances in mobile computing and multimedia applications demand high - performance and low - power VLSI digital signal processing (DSP) systems. One of the most widely used operations in DSP is finite - impulse response (FIR) filtering. In the existing method FIR filter is designed using array multiplier, which is having higher delay and power dissipation. The proposed method presents a programmable digital finite impulse response (FIR) filter for high - performance applications. One of the most widely used operations in DSP is finite - impulse response (FIR) filtering. In the existing method FIR filter is designed using array multiplier, which is having higher delay and power dissipation. The proposed method presents a programmable digital finite impulse response (FIR) filter for high performance applications. The FIR filter performs the weighted summations of input sequences and is widely used in video convolution functions, signal preconditioning, and various communication applications. Recently, due to the high - performance requirement and increasing complexity of DSP and multimedia communication application. In this work, , FIR filter multipliers are extensively characterized with power simulations, providing a methodology for the perturbation of the coefficients of baseline filters at the algorithm level to trade-off reduced power consumption for filter quality. The proposed optimization technique does not require any hardware overhead and it enables the possibility of scaling the power consumption of the filter at runtime.

1. Introduction

The proliferation of portable devices over the last decade, as well as the increasing interest in future Internet of Things (IoT) applications, have contributed to an increasing demand for near-sensor data analysis and filtering to reduce the amount of information to be wirelessly transmitted, which is key to reduce the consumed system energy. As near sensor signal processing now often becomes one of the most complex tasks of the system, programmable general-purpose platforms are required to support the requirements from different applications. In this scenario, possible solutions are software-programmable ultra-low power (ULP) architectures with dedicated, but reconfigurable accelerators for costly core computational kernels. Programmable finite impulse response (FIR) filters are one of the most widely implemented accelerators and they are a fundamental building block for many DSP applications. In addition, they are responsible for a relatively large portion of the power in the system as they are often a key kernel that might even continuously operate, for example to detect wake-up events. Therefore, it can be expected that methods for reducing their power consumption can have a large impact on a variety of IoT systems and applications.

The filter whose impulse response is finite, then it is said to be finite impulse response (FIR). As compared to IIR filter the FIR filter is more stable, feedback is not involved and higher order filtering. This FIR filter is non recursive, but the IIR filter is recursive. In DSP application the FIR filter is mostly used for their operation. The different methods are used to design the FIR filters, namely windowing method, Frequency sampling method, Weighted least square design and Equiripple FIR filters can be designed using the FFT algorithms as well. Analog filter is less expensive than digital filter due to their increased complexity. A binary multiplier plays vital role in digital electronics such as personal computer and to multiply two binary numbers

2. Literature review

FIR filtering is one of the most widely used operations performed in DSP applications. In this paper, a low power reconfigurable FIR filter is designed, in which the input data are monitored and the multipliers in the filter are disabled when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of the multipliers, significant power savings can be achieved with minor degradation in performance. An amplitude detector block is used to monitor the inputs of the filter. A control signal generator counts the number of inputs that have small amplitude and the multipliers are disabled only when consecutive inputs are small. The filter is designed using VHDL, simulated in Modelsim SE 5.7g and synthesized in Xilinx ISE 8.1. The results of conventional and the Reconfigurable FIR filter are compared.

Now a days the DSP processor essentially contain multipliers as its base element ,speed of the DSP processor depend on the speed of the multiplier. The addition, multiplication and signal delay which is necessary to design FIR filter. But it minimizes the operation speed and consumes some amount of power, area and delay. Sixteen sutras are in old fashioned Vedic mathematics out of them Urdhava Tiryakbhyam sutras and Nikhilam sutras are observed which is applied with FIR filter but the Nikhilam Navatascaramam Dasatah sutra is the popular calculation. This sutras is mainly used to multiply two numbers where elementary multiplication takes a excess time to multiply numbers and calculate the product but the Nikhilam sutras describes in base method is used to improve speed of the processor. The Urdhva Tiryakbhyam and Nikhilam sutra algorithms are compared in terms of power, time delay and area and found that Nikhilam sutra is faster for larger inputs than Urdhava Tiryakbhyam sutra

3. Existing Method

The BW2 multiplier is a simple structure which can achieve medium operating speed with moderate silicon area. Two n-bit input operands are passed to the PPG that implements the Baugh-Wooley scheme, which feeds the PPR implemented as a carry-save adder with (m,2) compressors. For the considered implementation, the half adders (HAs) and full adders (FAs) instantiated inside each of the compressors are connected in a tree structure to reduce the critical path of the PPR. The sums and carries of the PPR are then passed to the VMA implemented as a carry-propagate adder that provides the final result of the multiplication. The PPR is usually the most complex structure of the multiplier and therefore consumes the largest amount of power. For this reason, in order to reduce the power consumption of the BW2 multiplier, we first analyze the switching activity of the implemented PPR. The primary operation of the PPR is to shift and add the partial products, and therefore it is generally implemented with HAs and FAs as the main building blocks. The switching activity of these gates can be reduced by increasing the probability of having stable logic-zeros at their inputs, which corresponds to forcing more partial products to be equal to zero.

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Digital multipliers can be implemented choosing from a wide range of topologies based on the desired number representation, as well as on design requirements, such as area and speed [21]. Two of the most common topologies havebeen considered as an example for the analysis of theinternalswitching activity, which is strongly related to the dynamic power consumption: the radix-2 Baugh-Wooley (BW2) multiplier [22] that presents a simple and straight-forward implementation, and the radix-4 Booth-recoded (BR4) multiplier, known for its more complex structure and high-speed performance. Both topologies have been implemented to performsigned multiplication, using fixed-point two's complement asnumber representation. While these multipliers differ in the partial-products generator (PPG), they implement the same partial-products reducer (PPR) and the same vector-merging adder (VMA), here implemented as a carry-save adder with(m,2) compressors [22] and a carry-propagate adder, respectively.The RTL representations of both the BW2 multiplier and of the carry-save adder with (m,2) compressors have beentaken from the VHDL Library of Arithmetic Units proposedin [22]. The considered topologies are reviewed with more details in the following subsections.

3.1 Drawbacks

In the existing method FIR filter is designed using array multiplier, which is having higher delay and power dissipation

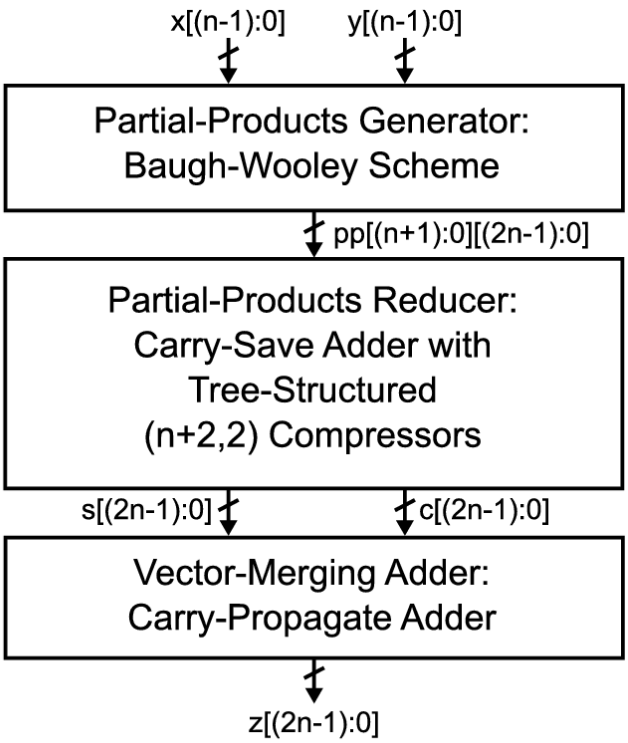

Fig. 1: Structure of signed n*n.bit radix*2 Baugh-Wooley multiplier

4. Proposed System

This technique can effectively be applied, as an example, to reconfigurable FIR accelerators. A simple greedy algorithm is used to modify the coefficients of a baseline filter to derive a new set of coefficients that are optimized for low power consumption while allowing for some degradation of the filtering quality. By exploiting the flexibility on the algorithm level, the proposed approximate computing technique does not require any design overhead for a programmable accelerator. At the same time, it ensures the quality of the baseline filter whenever it is required, while it offers also the possibility of scaling the power consumption at runtime when energy is short and reduced accuracy is tolerated. Since radix-2 Baugh-Wooley multipliers are rather slow, we also study a fast multiplier that uses Booth recoding. A BR4 multiplier has been considered where the PPR is fed with less than half of the partial products of those in the BW2 multiplier, thereby providing a much shorter critical path. As opposed to the symmetric BW2 multiplier, in the BR4 topology, the two input operands are processed differently, since x is passed to the recoding logic that decides which multiples of y should be fed to the PPR. For the considered implementation, a carry-save adder with (m,2) compressors is used for the PPR and a carry-propagate adder is used for the VMA, as in the BW2 multiplier.

. Partial product generation.

. A carry save adder (CSA) tree to reduce the partial products' matrix to an addition of only two operands.

. A carry propagation adder (CPA) for the final computation of the binary result.

In the design of a multiplier, the second module plays a pivotal role in terms of delay, power consumption and circuit complexity. Compressors have been widely used to speed up the CSA tree and decrease its power dissipation, so to achieve fast

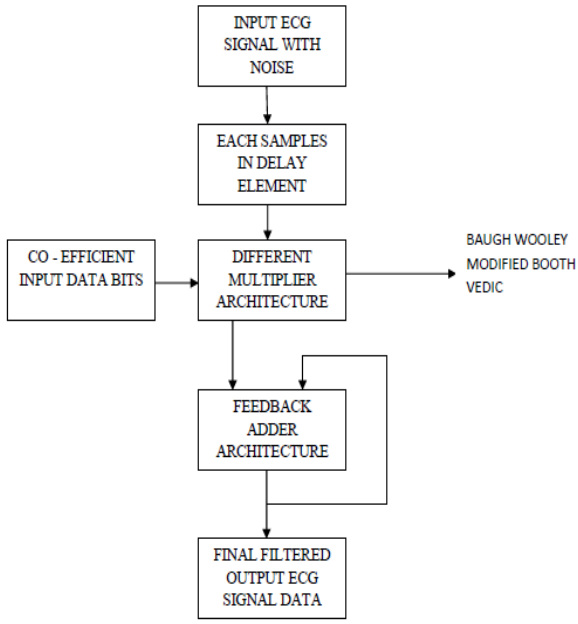

Fig.2: Low Power Multiplexed vedic Multiplier

5. Results

Simulation Results

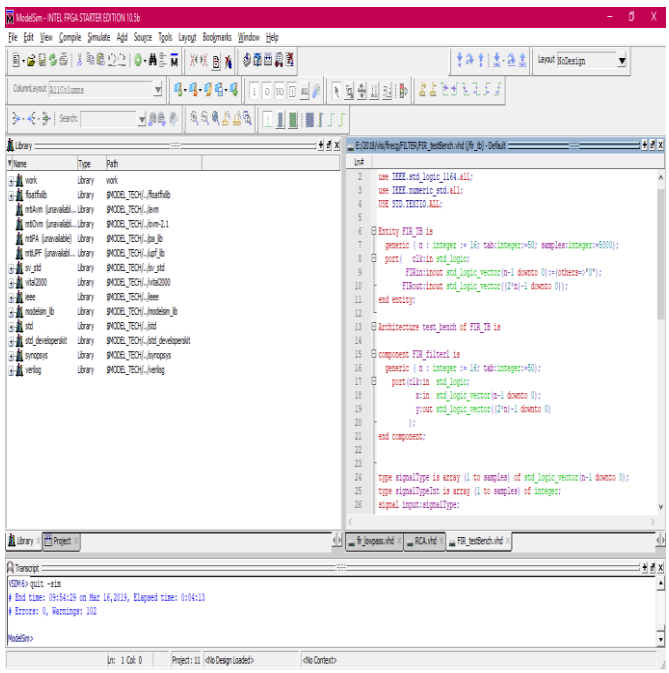

Fig. 3: Modalism editor window

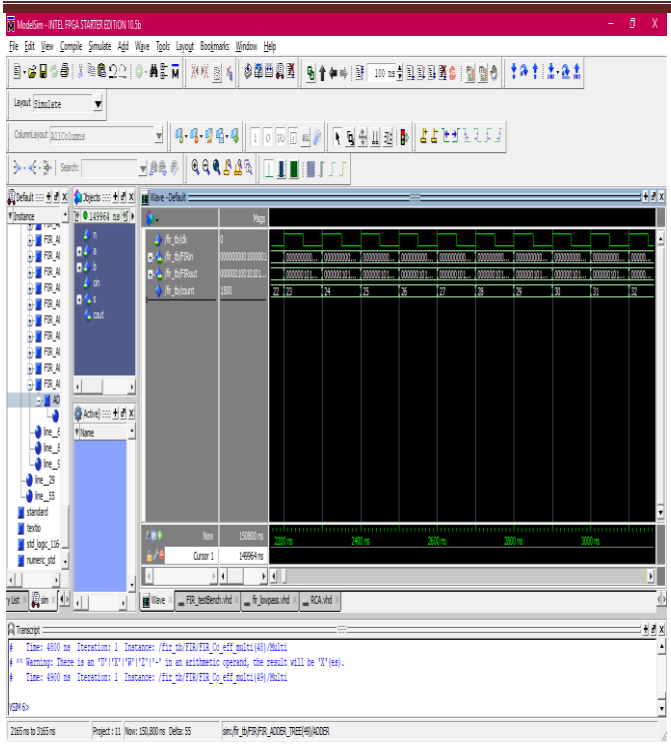

Fig.4: Vedic multiplier simulation waveform

6.Conclusions

Approximate multiplier for digital DSP 'Urdhava' and 'Tiryagbhyam' sutra words are derived from Sanskrit literature which means 'vertical and crosswise'. It is general multiplication formula applicable to different cases of multiplication. Urdhava Tiryagbhyam generates all partial products with concurrent addition of these partial products . Urdhava sutra is used in the generation of parallelism of partial product and their sums. This sutra can be generalized for N*N bit number. This multiplier is independent of clock frequency of the processor.

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